PATENT ABSTRACTS OF JAPAN

(54) VOLTAGE DETECTION CIRCUIT
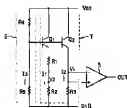
(57)Abstract:

PURPOSE: To obtain the circuit of simple circuit constitution which has good temperature characteristics of a detected voltage and is suitable for IC-implementation by applying the set voltage of a detected voltage setting circuit to the bases of two transistors(TR) of a band gap type reference voltage circuit. CONSTITUTION: The connection point of resistances R4 and R5 of the detected voltage setting circuit 2 is connected to the bases of the TRs Q1 and Q2 of the band gap type reference voltage circuit 1. When a source voltage VDD is applied, the output OUT of an operational amplifier circuit 3 rises while the emitter voltage V1 of the Q2 is lower than the voltage V2 at the connection point

of the resistances R1 and R2 and then falls when the VDD rises until the V1 becomes as high as the V2. In this case, the value of the DDD when V1=V2 is the detected voltage. This constitution makes the temperature characteristics of the detected voltage similar to those of a normal circuit and the pattern occupation area at the time of the IC-implementation is reducible.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] Each collector of the 1st transistor same type and the 2nd transistor is connected to the 1st potential edge, respectively. The series connection of the 1st resistance and resistance of the 2nd is carried out between the emitter of the 1st transistor of the above, and the 2nd potential edge. The band gap mold reference voltage circuit where it comes to connect the 3rd resistance between the emitter of the 2nd transistor of the above, and the above-mentioned 2nd potential edge, The detection electrical-potential-difference setting-out circuit where the series connection of the 4th resistance and resistance of the 5th was carried out between said 1st potential edges and 2nd potential edges, and the series-connection point was connected to each base of said 1st transistor and the 2nd transistor, One input edge is connected to the emitter of said 2nd transistor, and the input edge of another side is connected at the node of said 1st resistance and the 2nd resistance. The electrical-potential-difference detecting circuit characterized by providing the operation amplifying circuit which the time of carrying out the electrical-potential-difference comparison of both the inputs, and both inputs becoming equal is detected [amplifying circuit], and reverses a detection output.

[Claim 2] An electrical-potential-difference detecting circuit according to claim 1 is an electrical-potential-difference detecting circuit characterized by being used for the power-on clear circuit which is formed in a semiconductor integrated circuit, detects the power up of a semiconductor integrated circuit, and generates the signal for reset.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention is used for the power-on clear circuit which
starts the electrical-potential-difference detecting circuit formed in a
semiconductor integrated circuit, for example, detects a power up, and generates
the signal for reset.

[0002]

[Description of the Prior Art] The conventional electrical-potential-difference
detecting circuit used for a power-on clear circuit is constituted as shown in
drawing 5 or drawing 7 . That is, by consisting of one NPN transistor Q and three
resistance R1-R3, and one operation amplifying circuit OP, and comparing the
partial pressure electrical potential difference (detection electrical-potential-
difference programmed voltage) by resistance R2 and R3 with the electrical
potential difference VBE between base emitters of NPN transistor Q, supply
voltage VDD detects whether it started to the predetermined detection electrical
potential difference, and the electrical-potential-difference detecting circuit shown
in drawing 5 reverses the detection output OUT.

[0003] However, in the electrical-potential-difference detecting circuit of drawing

5 , since the partial pressure electrical potential difference has the temperature characteristic negative [**************] in VBE, as it shows the temperature characteristic to drawing 6 , the detection electrical potential difference VDD will have the negative temperature characteristic.

[0004] The band gap mold reference voltage circuit of the feedback control mold with which the electrical-potential-difference detecting circuit shown in drawing 7 consists of two NPN transistors Q1 and Q2, three resistance R1-R3, and an operation amplifying circuit OP1 for feedback controls on the other hand, It consists of an operation amplifying circuit OP2 for comparing the detection electrical-potential-difference programmed voltage by two resistance R4 and R5 for detection electrical-potential-difference setting out, and these two resistance R4 and R5 with the output voltage of said band gap mold reference voltage circuit, and the temperature characteristic of the detection electrical potential difference VDD can be set to about 0. In addition, the example of a circuit of the operation amplifying circuits OP1 and OP2 is shown in drawing 8 , and, as for P1-P4, a P channel MOS transistor, and N1-N3 are N-channel metal oxide semiconductor transistors.

[0005] However, the electrical-potential-difference detecting circuit shown in drawing 7 has many circuit elements, and since the pattern occupancy area of an operation amplifying circuit becomes quite large especially in case the operation amplifying circuits OP1 and OP2 whose number is two are needed and integrated-circuit-ized, it is unsuitable for integrated-circuit-izing.

[0006]

[Problem(s) to be Solved by the Invention] As described above, although it improves so that a detection electrical potential difference may not have the negative temperature characteristic, the conventional electrical-potential-difference detecting circuit needs many a circuit element and two operation amplifying circuits, and since pattern occupancy area becomes quite large in case it integrated-circuit-izes, it has the problem of being unsuitable for integrated-circuit-izing.

[0007] In case it integrated-circuit-izes, pattern occupancy area is comparatively small, and it was made that this invention should solve the above-mentioned trouble, ends [the object has the good temperature characteristic of a detection electrical potential difference, and circuitry is very easy, and], and is in offering the suitable electrical-potential-difference detecting circuit for integrated-circuit-izing.

[0008]

[Means for Solving the Problem] As for the electrical-potential-difference detecting circuit of this invention, each collector of the 1st transistor same type and the 2nd transistor is connected to the 1st potential edge, respectively. The series connection of the 1st resistance and resistance of the 2nd is carried out between the emitter of the 1st transistor of the above, and the 2nd potential edge. The band gap mold reference voltage circuit where it comes to connect the 3rd resistance between the emitter of the 2nd transistor of the above, and the above-mentioned 2nd potential edge, The detection electrical-potential-difference setting-out circuit where the series connection of the 4th resistance and resistance of the 5th was carried out between said 1st potential edges and 2nd potential edges, and the series-connection point was connected to each base of said 1st transistor and the 2nd transistor, It is characterized by providing the operation amplifying circuit which the time of one input edge being connected to the emitter of said 2nd transistor, and the input edge of another side being connected at the node of said 1st resistance and the 2nd resistance, carrying out the electrical-potential-difference comparison of both the inputs, and both inputs becoming equal is detected [amplifying circuit], and reverses a detection output.

[0009]

[Function] It becomes possible to improve the temperature characteristic of a detection electrical potential difference by giving the programmed voltage of a detection electrical-potential-difference setting-out circuit to each base of two transistors of a band gap mold reference voltage circuit, circuitry is very easy and only one for an electrical-potential-difference comparison needs an operation

amplifying circuit, but in case it integrated-circuit-izes, pattern occupancy area is comparatively small and it ends, and it is suitable for integrated-circuit-izing.

[0010]

[Example] Hereafter, one example of this invention is explained to a detail with reference to a drawing.

[0011] The electrical-potential-difference detecting circuit used for the power-on clear circuit which drawing 1 is formed in a semiconductor integrated circuit, detects the power up of a semiconductor integrated circuit, and generates the signal for reset is shown, and, as for a band gap mold reference voltage circuit and 2, 1 is [a detection electrical-potential-difference setting-out circuit and 3] operation amplifying circuits.

[0012] As for the above-mentioned band gap mold reference voltage circuit 1, each collector of the 1st transistor Q1 same type (this example NPN) and the 2nd transistor Q2 is connected to the 1st potential edge (this example power-source potential VDD), respectively. The series connection of the 1st resistance R1 and the resistance R2 of the 2nd is carried out between the emitter of the 1st transistor Q1 of the above, and the 2nd potential edge (this example touch-down potential GND), and it comes to connect the 3rd resistance R3 between the emitter of the 2nd transistor Q2 of the above, and the above-mentioned 2nd potential edge.

[0013] Moreover, the series connection of the 4th resistance R4 and the resistance R5 of the 5th is carried out between said 1st potential edges and 2nd potential edges, and, as for the above-mentioned detection electrical-potential-difference setting-out circuit 2, the node is connected to each base of said 1st transistor Q1 and the 2nd transistor Q2.

[0014] Moreover, as for the above-mentioned operation amplifying circuit 3, one input edge (this example - input edge) is connected to the emitter of said 2nd transistor Q2. The time of the input edge (this example + input edge) of another side being connected at the node of said 1st resistance R1 and the 2nd resistance R2, carrying out the electrical-potential-difference comparison of both

the inputs, and both inputs becoming equal is detected, and the detection output OUT (auto clear signal) is reversed. Next, it explains, referring to drawing 2 about actuation of the electrical-potential-difference detecting circuit of the above-mentioned configuration.

[0015] The electrical potential difference of the node of the 4th resistance R4 and the 5th resistance R5 VREF, VBE1 and the electrical potential difference between base emitters of the 2nd transistor Q2 for the electrical potential difference between base emitters of the 1st transistor Q1 VBE2, When the electrical potential difference of the node of V1, the 1st resistance R1, and the 2nd resistance R2 is expressed with V2, change of each part electrical potential difference to change of supply voltage VDD comes to show the emitter electrical potential difference of the 2nd transistor Q2 to drawing 2 . namely, electrical potential difference VREF an electrical potential difference VDD carries out a partial pressure by the 4th resistance R1 and the resistance R5 of the 5th -- having -- an electrical potential difference V1 -- the above-mentioned electrical potential difference VREF VBE2 only -- low -- an electrical potential difference V2 -- the above-mentioned electrical potential difference VREF -- VBE1 only -- the partial pressure of the low electrical potential difference is carried out by the 1st resistance R1 and the resistance R2 of the 2nd.

[0016] In the above-mentioned electrical-potential-difference detecting circuit, if supply voltage VDD is switched on, when supply voltage VDD starts until the output OUT of the operation amplifying circuit 3 starts and it is set to V1=V2 between V1<V2, the output OUT of the operation amplifying circuit 3 will fall. in this case, the value of the supply voltage VDD when being set to V1=V2 -- detection electrical potential difference VACL it is .

[0017] Next, the property of the above-mentioned electrical-potential-difference detecting circuit is analyzed. if the current which flows the current which flows the current which flows the emitter surface ratio of the 1st transistor Q1 and the 2nd transistor Q2 to N:1 and the 2nd resistance to I1 and the 3rd resistance R3 to I2 and the 5th resistance R5 is expressed with I3 -- the following formulas (1-1) --

and (1-2) it is materialized.

[0018]

[Equation 1]

$$(V_{REF} - V_{BE1}) \cdot \frac{R_2}{R_1 + R_2} = V_{REF} - V_{BE2} \qquad \cdots (1\text{-}1)$$

$$V_{REF} = (V_{BE2} - V_{BE1} \cdot \frac{R_2}{R_1 + R_2}) \div (1 - \frac{R_2}{R_1 + R_2})$$

$$= \frac{V_{BE2} \cdot (R_1 + R_2) - V_{BE1} \cdot R_2}{R_1}$$

$$= V_{BE2} + \frac{R_2}{R_1} (V_{BE2} - V_{BE1})$$

$$= V_{BE2} + \frac{R_2}{R_1} (V_T \cdot \ell n \frac{I_2}{I_S} - V_T \cdot \ell n \frac{I_1}{I_S \cdot N})$$

$$= V_{BE2} + \frac{R_2}{R_1} (V_T \cdot \ell n \frac{I_2 \cdot N}{I_1}) \qquad \cdots (1\text{-}2)$$

[0019] However, VT It is the pyrovoltage expressed with $V_T = k \cdot T/q$, and k is [absolute temperature and q of a Boltzmann's constant (1.38x10-23 j/) and T] the amounts of electronic charge (1.60x10-19 coulomb). At the time of V1=V2, it is I1 and R2=I2, and R3 here. -- (2-1)

A next door, I2/I1=R2/R1 -- (2-2)

It comes out, it is, and if a formula (2-2) is substituted for a formula (1-2), the following (3) types will be obtained.

[0020]

[Equation 2]

$$V_{REF} = V_{BE2} + \frac{R_2}{R_1} V_T \cdot \ell n \frac{R_2 \cdot N}{R_3} \qquad \cdots (3)$$

Next, detection electrical potential difference VACL It asks.

[0021]

[Equation 3]

$$V_{REF} = \frac{R_5}{R_4 + R_5} V_{ACL} \qquad \cdots (4-1)$$

$$V_{ACL} = \frac{R_4 + R_5}{R_5} V_{REF} = (\frac{R_4}{R_5} + 1) \ V_{REF} \qquad \cdots (4-2)$$

(3) Substitute a formula for a formula (4-2).

[0022]

[Equation 4]

$$V_{ACL} = (\frac{R_4}{R_5} + 1)(V_{BE2} + \frac{R_2}{R_1} V_T \cdot \ell \, n \frac{R_2 \cdot N}{R_3}) \qquad \cdots (5)$$

Next, detection electrical potential difference VACL The temperature characteristic is searched for.

[0023]

[Equation 5]

$$\frac{\partial V_{BE2}}{\partial T} \approx -2 \, mV / ℃ \qquad \cdots (6)$$

$$\frac{\partial V_T}{\partial T} = 0.086 \, mV / ℃ \qquad \cdots (7)$$

It shall carry out and dispersion and the temperature characteristic of resistance (for example, diffused resistor) R4 and R5 shall carry out ****** disregard.

[0024]

[Equation 6]

$$\frac{\partial V_{REF}}{\partial T} \approx 0 \, mV / ℃$$

It is [0025] in order to carry out.

[Equation 7]

$$\frac{\partial V_{REF}}{\partial T} \simeq -2 + 0.086 \ (\frac{R_2}{R_1} \ell n \ \frac{R_2 \cdot N}{R_3}) = 0 \qquad \cdots (8)$$

$$\therefore \quad \frac{R_2}{R_1} \ell n \ \frac{R_2 \cdot N}{R_3} = \frac{2}{0.086} \qquad \cdots (9)$$

What is necessary is for it to be alike and just to design. Thus, detection electrical potential difference VACL at the time of designing The result of having surveyed the temperature characteristic is shown in drawing 3 , and it has the slightly negative temperature characteristic.

[0026] According to the electrical-potential-difference detecting circuit of the above-mentioned example, namely, by giving the programmed voltage of a detection electrical-potential-difference setting-out circuit to each base of two transistors of a band gap mold reference voltage circuit It becomes possible to improve the temperature characteristic of a detection electrical potential difference to the circuit and equivalent extent of drawing 7 of the conventional example. Compared with the circuit of drawing 7 of the conventional example, circuitry becomes very easy, and only one for an electrical-potential-difference comparison needs an operation amplifying circuit, but in case it integrated-circuit-izes, pattern occupancy area is comparatively small and it ends, and it is suitable for integrated-circuit-izing.

[0027] In addition, if the value of resistance R1-R3 and the emitter surface ratio N of transistors Q1 and Q2 are adjusted in the above-mentioned example, it will be the detection electrical potential difference VACL. It becomes possible to set the temperature characteristic as forward or negative.

[0028] Moreover, drawing 4 makes reverse connection relation between supply voltage VDD and the touch-down potential GND while changing into PNP transistorQ1' and Q2' NPN transistors Q1 and Q2 of the electrical-potential-difference detecting circuit which shows the modification of the electrical-potential-difference detecting circuit shown in drawing 1 , and was shown in drawing 1 , and it gives the same sign to the same part as the inside of drawing

1 .

[0029]

[Effect of the Invention] As mentioned above, according to this invention, the temperature characteristic of a detection electrical potential difference is good, circuitry is very easy, in case it integrated-circuit-izes, pattern occupancy area is comparatively small, it ends, and the suitable electrical-potential-difference detecting circuit for integrated-circuit-izing can be realized.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The circuit diagram showing one example of the electrical-potential-difference detecting circuit of this invention.

[Drawing 2] Property drawing shown in order to explain actuation of the circuit of drawing 1 ,

[Drawing 3] Drawing showing an example of the detection voltage characteristic of the circuit of drawing 1 .

[Drawing 4] The circuit diagram showing the modification of the circuit of drawing 1 .

[Drawing 5] The circuit diagram showing the conventional electrical-potential-difference detecting circuit.

[Drawing 6] Drawing showing the detection voltage characteristic of the circuit of drawing 5 .

[Drawing 7] The circuit diagram showing the conventional electrical-potential-difference detecting circuit.

[Drawing 8] The circuit diagram showing an example of the operation amplifying circuit in the circuit of drawing 7 .

[Description of Notations]

1 -- a band gap mold reference voltage circuit, 2 -- detection electrical-potential-difference setting-out circuit, 3 -- operation amplifying circuit, Q1, and the -- 1st transistor, and Q1'Q2, Q2' -- the 2nd transistor, R1 -- the 1st resistance, R2 -- the 2nd resistance, and R3 -- the 3rd resistance, R4 -- the 4th resistance, and R5 -- the 5th resistance.

[Translation done.]

DRAWINGS

[Drawing 1]

[Drawing 2]

[Drawing 3]

[Drawing 4]

R5 R2 R3
3
OUT
R1
Q1 Q'2
R4
VDD
GND

[Drawing 5]

VDD
Q R2 OP
OUT
R1 R3
GND

[Drawing 6]

檢知電壓
(VACL)

[V]
4.0
3.0
2.0

-40   0   40   80 [℃]

温　度
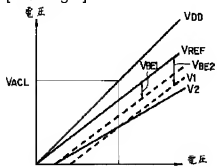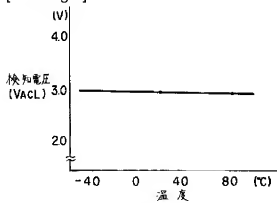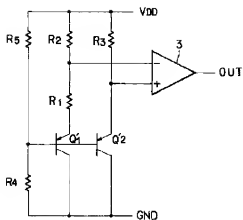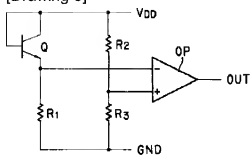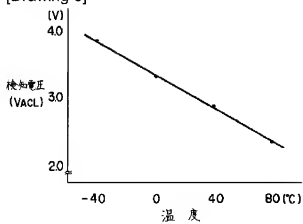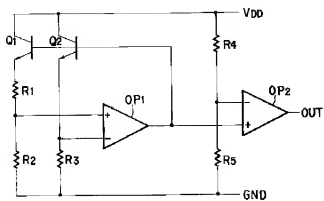
[Drawing 7]

[Drawing 8]

[Translation done.]

(54)【発明の名称】　電圧検知回路

(57)【要約】

【目的】　リセット信号を発生する際に、検知電圧の温度特性が良く、回路構成を簡単にできる電圧検知回路を提供することを目的とする。

【構成】　トランジスタQ1およびトランジスタQ2の各コレクタが電源電位VDDに接続され、トランジスタQ1のエミッタと接地電位GNDとの間に抵抗R1および抵抗R2が直列接続され、第2のトランジスタQ2のエミッタと接地電位GNDとの間に抵抗R3が接続されている。また、電源電位VDDと接地電位GNDとの間に抵抗R4および抵抗R5が直列接続され、その接続点がトランジスタQ1およびQ2の各ベースに接続されている。さらにトランジスタQ2のエミッタに演算増幅回路3の−入力端が接続され、抵抗R1および抵抗R2の接続点に演算増幅回路3の＋入力端が接続され、両入力が演算増幅回路3で比較される。
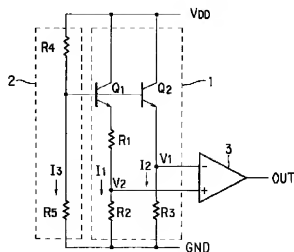
【特許請求の範囲】

【請求項1】 それぞれ同一タイプの第1のトランジスタおよび第2のトランジスタの各コレクタが第1電位端に接続され、上記第1のトランジスタのエミッタと第2電位端との間に第1の抵抗および第2の抵抗が直列接続され、上記第2のトランジスタのエミッタと上記第2電位端との間に第3の抵抗が接続されてなるバンドギャップ型基準電圧回路と、

前記第1電位端と第2電位端との間に第4の抵抗および第5の抵抗が直列接続され、その直列接続点が前記第1のトランジスタおよび第2のトランジスタの各ベースに接続された検知電圧設定回路と、

前記第2のトランジスタのエミッタに一方の入力端が接続され、前記第1の抵抗および第2の抵抗の接続点に他方の入力端が接続され、両入力を電圧比較して両入力が等しくなった時を検知して検知出力を反転させる演算増幅回路とを具備することを特徴とする電圧検知回路。

【請求項2】 請求項1記載の電圧検知回路は、半導体集積回路に形成され、半導体集積回路の電源投入時を検知してリセット用信号を生成するパワー・オン・クリア回路に使用されることを特徴とする電圧検知回路。

【発明の詳細な説明】

【0001】

【産業上の利用分野】 本発明は、半導体集積回路に形成される電圧検知回路に係り、例えば電源投入時を検知してリセット用信号を生成するパワーオン・クリア回路に使用される。

【0002】

【従来の技術】 パワーオン・クリア回路に使用される従来の電圧検知回路は、図5あるいは図7に示すように構成されている。即ち、図5に示す電圧検知回路は、1個のNPNトランジスタQと3個の抵抗R1～R3と1個の演算増幅回路OPとからなり、抵抗R2およびR3による分圧電圧（検知電圧設定電圧）とNPNトランジスタQのベース・エミッタ間電圧VBEとを比較することにより、電源電圧VDDが所定の検知電圧まで立ち上ったか否かを検知して検知出力OUTを反転させる。

【0003】 しかし、図5の電圧検知回路においては、分圧電圧は温度特性を殆んど持たないが、VBEは負の温度特性を持っているので、図6に示すように、検知電圧VDDが負の温度特性を持ってしまう。

【0004】 一方、図7に示す電圧検知回路は、2個のNPNトランジスタQ1、Q2と3個の抵抗R1～R3と帰還制御用の演算増幅回路OP1とからなる帰還制御型のバンドギャップ型基準電圧回路と、検知電圧設定用の2個の抵抗R4およびR5と、この2個の抵抗R4およびR5による検知電圧設定電圧と前記バンドギャップ型基準電圧回路の出力電圧とを比較するための演算増幅回路OP2とからなり、検知電圧VDDの温度特性をほぼ零にすることができる。なお、演算増幅回路OP1、O

P2の回路図を図8に示しており、P1～P4はPチャネルMOSトランジスタ、N1～N3はNチャネルMOSトランジスタである。

【0005】 しかし、図7に示す電圧検知回路は、回路素子数が多く、2個の演算増幅回路OP1、OP2を必要とし、集積回路化する際に特に演算増幅回路のパターン占有面積がかなり大きくなるので、集積回路化に不向きである。

【0006】

【発明が解決しようとする課題】 上記したように従来の電圧検知回路は、検知電圧が負の温度特性を持たないように改善するのに、多くの回路素子と演算増幅回路を2個必要とし、集積回路化する際にパターン占有面積がかなり大きくなるので集積回路化に不向きであるという問題がある。

【0007】 本発明は、上記問題点を解決すべくなされたもので、その目的は、検知電圧の温度特性が良く、回路構成が至って簡単であり、集積回路化する際にパターン占有面積が比較的小さくて済み、集積回路化に好適な電圧検知回路を提供することにある。

【0008】

【課題を解決するための手段】 本発明の電圧検知回路は、それぞれ同一タイプの第1のトランジスタおよび第2のトランジスタの各コレクタが第1電位端に接続され、上記第1のトランジスタのエミッタと第2電位端との間に第1の抵抗および第2の抵抗が直列接続され、上記第2のトランジスタのエミッタと上記第2電位端との間に第3の抵抗が接続されてなるバンドギャップ型基準電圧回路と、前記第1電位端と第2電位端との間に第4の抵抗および第5の抵抗が直列接続され、その直列接続点が前記第1のトランジスタおよび第2のトランジスタの各ベースに接続された検知電圧設定回路と、前記第2のトランジスタのエミッタに一方の入力端が接続され、前記第1の抵抗および第2の抵抗の接続点に他方の入力端が接続され、両入力を電圧比較して両入力が等しくなった時を検知して検知出力を反転させる演算増幅回路とを具備することを特徴とする。

【0009】

【作用】 検知電圧設定回路の設定電圧をバンドギャップ型基準電圧回路の2個のトランジスタのベースに与えることにより検知電圧の温度特性を改善することが可能になり、回路構成が至って簡単であり、演算増幅回路は電圧比較用に1個しか必要とせず、集積回路化する際にパターン占有面積が比較的小さくて済み、集積回路化に好適である。

【0010】

【実施例】 以下、図面を参照して本発明の一実施例を詳細に説明する。

【0011】 図1は、半導体集積回路に形成されて半導体集積回路の電源投入を検知してリセット用信号を生

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成するパワーオン・クリア回路に使用される電圧検知回路を示しており、1はバンドギャップ型基準電圧回路、2は検知電圧設定回路、3は演算増幅回路である。

【0012】上記バンドギャップ型基準電圧回路1は、それぞれ同一タイプ（本例ではNPN）の第1のトランジスタQ1および第2のトランジスタQ2の各コレクタが第1電位端（本例では電源電位VDD）に接続され、上記第1のトランジスタQ1のエミッタと第2電位端（本例では接地電位GND）との間に第1の抵抗R1および第2の抵抗R2が直列接続され、上記第2のトランジスタQ2のエミッタと上記第2電位端との間に第3の抵抗R3が接続されてなる。

【0013】また、上記検知電圧設定回路2は、前記第1電位端と第2電位端との間に第4の抵抗R4および第5の抵抗R5が直列接続され、その接続点が前記第1のトランジスタQ1および第2のトランジスタQ2の各ベースに接続されている。

【0014】また、上記演算増幅回路3は、前記第2のトランジスタQ2のエミッタに一方の入力端（本例では−入力端）が接続され、前記第1の抵抗R1および第2の抵抗R2の接続点に他方の入力端（本例では＋入力端）が接続され、両入力を電圧比較して両入力が等しくなった時を検知して検知出力OUT（オートクリア信号）を反転させる。次に、上記構成の電圧検知回路の動作を図2を参照しながら説明する。

【0015】第4の抵抗R4および第5の抵抗R5の接*

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*続点の電圧をVREF、第1のトランジスタQ1のベース・エミッタ間電圧をVBE1、第2のトランジスタQ2のベース・エミッタ間電圧をVBE2、第2のトランジスタQ2の抵抗R2の接続点の電圧をV2で表わすと、電源電圧VDDの変化に対する各部電圧の変化は図2に示すようになる。即ち、電圧VREFは電圧VDDが第4の抵抗R1および第5の抵抗R5により分圧されたものであり、電圧V1は上記電圧VREFよりVBE2だけ低く、電圧V2は電圧VREFよりVBE1だけ低い電圧が第1の抵抗R1および第2の抵抗R2により分圧されたものである。

【0016】上記電圧検知回路においては、電源電圧VDDが投入されると、V1＜V2の間は演算増幅回路3の出力OUTが立ち上がり、V1＝V2になるまで電源電圧VDDが立ち上がった時に演算増幅回路3の出力OUTが立ち下がる。上記V1＝V2になった時の電源電圧VDDの値が検知電圧VACLである。

【0017】次に、上記電圧検知回路の特性を解析する。第1のトランジスタQ1および第2のトランジスタQ2のエミッタ面積比をN：1、第2の抵抗に流れる電流をI1、第3の抵抗R3に流れる電流をI2、第5の抵抗R5に流れる電流I3で表わすと、以下の式（1−1）及び（1−2）が成立する。

【0018】

【数1】

$$(V_{REF} - V_{BE1}) \cdot \frac{R_2}{R_1 + R_2} = V_{REF} - V_{BE2} \quad \cdots (1 \cdot 1)$$

$$V_{REF} = (V_{BE2} - V_{BE1} \cdot \frac{R_2}{R_1 + R_2}) \div (1 - \frac{R_2}{R_1 + R_2})$$

$$= \frac{V_{BE2} \cdot (R_1 + R_2) - V_{BE1} \cdot R_2}{R_1}$$

$$= V_{BE2} + \frac{R_2}{R_1} (V_{BE2} - V_{BE1})$$

$$= V_{BE2} + \frac{R_2}{R_1} (V_T \cdot \ln \frac{I_2}{I_S} - V_T \cdot \ln \frac{I_1}{I_S \cdot N})$$

$$= V_{BE2} + \frac{R_2}{R_1} (V_T \cdot \ln \frac{I_2 \cdot N}{I_1}) \quad \cdots (1-2)$$

【0019】ただしVTはVT＝k・T/qで表される熱電圧であり、kはボルツマン定数（1.38×10⁻²³ J/）、Tは絶対温度、qは電子の電荷量（1.60×10⁻¹⁹ クーロン）である。ここでV1＝V2のときには、

I1・R2＝I2・R3…（2−1）
となり、
I2／I1＝R2／R1…（2−2）
であり、（2−2）式を（1−2）式に代入すると次の（3）式が得られる。

【0020】

【数2】

$$V_{REF} = V_{BE2} + \frac{R_2}{R_1} V_T \cdot \ell n \frac{R_2 \cdot N}{R_3} \quad \cdots (3)$$

次に、検知電圧VACLを求める。

【数3】

【0021】

$$V_{REF} = \frac{R_5}{R_4 + R_5} V_{ACL} \quad \cdots (4-1)$$

$$V_{ACL} = \frac{R_4 + R_5}{R_5} V_{REF} = \left(\frac{R_4}{R_1} + 1\right) V_{REF} \quad \cdots (4-2)$$

（3）式を（4−2）式に代入する。

【数4】

【0022】

$$V_{ACL} = \left(\frac{R_4}{R_5} + 1\right)\left(V_{BE2} + \frac{R_2}{R_1} V_T \cdot \ell n \frac{R_2 \cdot N}{R_3}\right) \quad \cdots (5)$$

次に、検知電圧VACLの温度特性を求める。

【数5】

【0023】

$$\frac{\partial V_{BE2}}{\partial T} \simeq -2 \, mV/℃ \quad \cdots (6)$$

$$\frac{\partial V_T}{\partial T} = 0.086 \, mV/℃ \quad \cdots (7)$$

とし、抵抗（例えば拡散抵抗）R4、R5のばらつきや温度特性は殆んど無視し得るものとする。

【0024】

【数6】

$$\frac{\partial V_{REF}}{\partial T} \simeq 0 \, mV/℃$$

とするためには、

【0025】

【数7】

$$\frac{\partial V_{REF}}{\partial T} \simeq -2 + 0.086 \left(\frac{R_2}{R_1} \ell n \frac{R_2 \cdot N}{R_3}\right) = 0 \quad \cdots (8)$$

$$\therefore \frac{R_2}{R_1} \ell n \frac{R_2 \cdot N}{R_3} = \frac{2}{0.086} \quad \cdots (9)$$

に設計すればよい。このように設計した場合の検知電圧VACLの温度特性を実測した結果を図3に示しており、僅かながら負の温度特性を持っている。

【0026】即ち、上記実施例の電圧検知回路によれば、検知電圧設定回路の設定電圧をバンドギャップ型基準電圧回路の2個のトランジスタの各ベースに与えることにより、検知電圧の温度特性を従来例の図7の回路と同等程度に改善することが可能になり、従来例の図7の回路と比べて回路構成が至って簡単になり、演算増幅回路は電圧比較用の1個しか必要とせず、集積回路化する際にパターン占有面積が比較的小さくて済み、集積回路化

化に好適である。

【0027】なお、上記実施例において、抵抗R1〜R3の値、トランジスタQ1、Q2のエミッタ面積比Nを調整すれば、検知電圧VACLの温度特性を正または負に設定することが可能になる。

【0028】また、図4は、図1に示した電圧検知回路の変形例を示しており、図1に示した電圧検知回路のNPNトランジスタQ1、Q2をPNPトランジスタQ1'、Q2'に変更すると共に電源電圧VDDと接地電位GNDとの接続関係を逆にしたものであり、図1中と同一部分には同一符号を付している。

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【0029】
【発明の効果】上述したように本発明によれば、検知電圧の温度特性が良く、回路構成が至って簡単であり、集積回路化する際にパターン占有面積が比較的小さくて済み、集積回路化に好適な電圧検知回路を実現することができる。
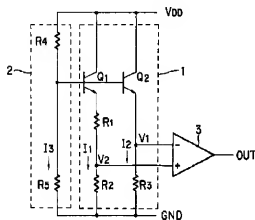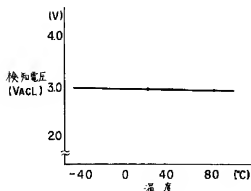【図面の簡単な説明】
【図1】本発明の電圧検知回路の一実施例を示す回路図。
【図2】図1の回路の動作を説明するために示す特性図。
【図3】図1の回路の検知電圧特性の一例を示す図。

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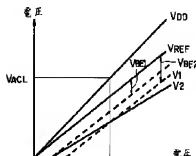【図4】図1の回路の変形例を示す回路図。
【図5】従来の電圧検知回路を示す回路図。
【図6】図5の回路の検知電圧特性を示す図。
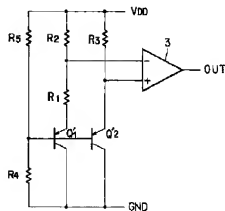【図7】従来の電圧検知回路を示す回路図。
【図8】図7の回路中の演算増幅回路の一例を示す回路図。
【符号の説明】
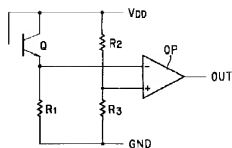1…バンドギャップ型基準電圧回路、2…検知電圧設定回路、3…演算増幅回路、Q1、Q1′…第1のトランジスタ、Q2、Q2′…第2のトランジスタ、R1…第1の抵抗、R2…第2の抵抗、R3…第3の抵抗、R4…第4の抵抗、R5…第5の抵抗。
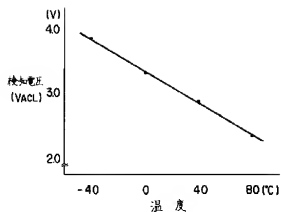
【図1】

【図2】

【図3】

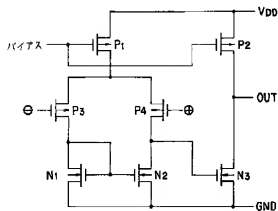
【図4】

【図5】

【図6】

【図7】

【図8】